REMARKS/ARGUMENTS

Introduction

Claims 1-8 and 10-17 are rejected under 35 U.S.C. §103(a) as being unpatentable over Cohen (US Patent No. 5,751,614) in view of Deip (article entitled Performance Evaluation of the PowerPC 620 Microstructure). Claim 9 and 18 are rejected under 35 U.S.C. §103(a) as being unpatentable over Cohen in view of Deip as applied to claims 1-8, 10-17, and further in view of Kabir (US Patent No. 6,538,657). Claims 1-32 are pending. Claims 1-18 remain unchanged, and new claims 19-32 have been added.

Applicants would like to thank the Examiner for acknowledging the Information Disclosure Statements and Forms 1449 filed on June 10, 2005 and February 1, 2006 by providing a signed copy of the 1449 forms. However, the Examiner has not provided a signed copy of the Information Disclosure Statements and Forms 1449 filed concurrently with the patent application on January 15, 2004. Applicants have provided a copy of these papers and the post card acknowledging their receipt. Applicants respectfully request that the Examiner acknowledge these papers and provide a signed copy of the Forms 1449 to Applicants with the next Office Action.

Rejection of Claims Under 35 U.S.C. § 103

Regarding the obviousness rejections, each of the three references (Cohen, Diep, and Kabir) cited by the Examiner fails to qualify as prior art to the pending claims. The present application claims priority back to the 8/16/95 filing date of U.S. Patent Application No. 08/516,036, which issued into U.S. Patent No. 5,742,840 (the '840 patent). This chain of priority also includes a continuation-in-part application, U.S. Patent Application No. 09/382,402, which issued into U.S. Patent no. 6,295,599 (the '599 patent). The priority claim is hereby reproduced for the convenience of the Examiner:

> This application is a continuation of U.S. patent application Ser. No. 10/646,787, filed Aug. 25, 2003, which is a continuation of U.S. patent application Ser. No. 09/922,319, filed Aug. 2, 2001, which is a continuation of U.S. patent application Ser. No. 09/382,402, filed Aug. 24,

1999, now U.S. Pat. No. 6,295,599, which claims the benefit of priority to Provisional Application No. 60/097,635 filed Aug. 24, 1998, and is a continuation-in-part of U.S. patent application Ser. No. 09/169,963, filed Oct. 13, 1998, now U.S. Pat. No. 6,006,318, which is a continuation of U.S. patent application Ser. No. 08/754,827, filed Nov. 22, 1996 now U.S. Pat. No. 5,822,603, which is a divisional of U.S. patent application Ser. No. 08/516,036, filed Aug. 16, 1995 now U.S. Pat. No. 5,742,840.

Cohen fails to qualify as prior art because the earliest filing date of Cohen associated with the feature cited by the Examiner is 2/29/96. The Examiner cites to the "mask" feature in Fig. 3 of Cohen. Cohen is a continuation-in-part (CIP) of parent application 08/444,814, filed 5/18/95. However, the "mask" feature cited by the Examiner was not disclosed in the parent application. That is, the "mask" feature appeared for the first time in the Cohen application filed 2/29/96, which is after the 8/16/95 priority date of the present application. As such, Cohen fails to qualify as prior art against the pending claims.

Diep also fails to qualify as prior art against the pending claims. Diep is a paper that appears to have been published in 1995. See Diep, copyright notice dated 1995. Thus, Diep was not published more than one year prior to the 8/16/95 priority date of the present application. As such, Diep fails to qualify as prior art against the pending claims.

Finally, Kabir fails to qualify as prior art against the pending claims. Kabir is a continuation of parent application Ser. No. 09/289,783, filed 4/9/99, which is a continuation of application. 08/563,059, filed 11/27/95. Thus, Kabir was filed after the 8/16/95 priority date of the present application and fails to qualify as prior art against the pending claims.

The obviousness rejections rely on the three references Cohen, Diep, and Kabir, all of which fail to qualify as prior art against the pending claims. As such, the obviousness rejections cannot stand, and claims 1-8 and 10-17 are patentable over the cited references.

Support for Pending Claims 1-18

As mentioned above, the priority date of 8/16/95 of the present application is established through a claim of priority that includes the '840 patent and its appendix (the '840 appendix) and the '599 patent and its appendix (the '599 appendix). Support for pending claims 1-32 is found in the '840 patent, '840 appendix, '599 patent, and the '599 appendix is presented below.

Regarding claim 1, a programmable processor comprising in part "an instruction path; a data path; an external interface operable to receive data from an external source and communicate the received data over the data path; a register file operable to receive and store data from the data path and communicate the stored data to the data path; and an execution unit coupled to the instruction and data paths and operable to decode and execute instructions received from the instruction path" is described in the '599 patent at Fig. 1 and col. 4, lines 10-66, and the '840 patent at Figures 6 and 7, and col. 11, line 19 through col. 13, line 11.

Regarding claim 1, the recited programmable processor further comprising in part an execution unit "wherein in response to decoding a single instruction specifying both a mask and a register containing data, the mask comprising fields that each correspond to a field of the data contained in the register, the execution unit is operable to: (i) detect some of the fields of the mask as having a predetermined value and identifying corresponding fields of the data contained in the register as write-enabled data fields; and (ii) cause the write-enabled data fields to be written to a specified memory location" is described in the '599 appendix at p. 123-25 and 128-30, and the '840 appendix at p. 150-53 and 154-57.

Regarding claim 2, the recited programmable processor "each of the fields of the mask has a width of one bit" is described in the '599 appendix at p. 123-25 and 128-30, and the '840 appendix at p. 150-53 and 154-57.

Regarding claim 3, the recited programmable processor "wherein each of the fields of the data contained in the register has a width of one bit" is described in the '599 appendix at p. 123-25 and 128-30, and the '840 appendix at p. 150-53 and 154-57.

Regarding claim 4, the recited programmable processor "wherein the execution unit is operable to cause the write-enabled data fields to be written to the specified memory location by reading an unaltered field of data from the specified memory location and writing the unaltered field of data along with the write-enabled data fields to the specified memory location" is described in the '599 appendix at p. 123-25 and 128-30, and the '840 appendix at p. 150-53 and 154-57.

Regarding claim 5, the recited programmable processor "wherein the mask is contained in a specified register" is described in the '599 appendix at p. 123-25 and 128-30, and the '840 appendix at p. 150-53 and 154-57.

Regarding claim 6, the recited programmable processor "wherein the memory location is contained in a specified register" is described in the '599 appendix at p. 123-25 and 128-30, and the '840 appendix at p. 150-53 and 154-57.

Regarding claim 7, the recited programmable processor "wherein the specified memory location comprises a section of memory having a specific width and beginning at a specific memory address" is described in the '599 appendix at p. 123-25 and 128-30, and the '840 appendix at p. 150-53 and 154-57.

Regarding claim 8, the recited programmable processor "wherein the predetermined value is a logic 1" is described in the '599 appendix at p. 123-25 and 128-30, and the '840 appendix at p. 150-53 and 154-57.

Regarding claim 9, the recited programmable processor "wherein the execution unit is further operable to, in response to decoding a second single instruction specifying a third and a fourth register each containing a plurality of operands, multiply the plurality of floating point operands in the third register by the plurality of operands in the fourth register to produce a plurality of products and provide the plurality of products to partitioned fields of a result register as a second catenated result" is described in the '599 appendix at p. 258-60, and the '840 appendix at p. 129-131.

Regarding claim 10, a data processing system comprising in part "(a) a bus coupling components in the data processing system; (b) an external memory coupled to the bus; (c) a programmable microprocessor coupled to the bus and capable of operation independent of another host processor, the microprocessor comprising: an instruction path; a data path; an external interface operable to receive data from an external source and communicate the received data over the data path; a register file operable to receive and store data from the data path and communicate the stored data to the data path; and an execution unit coupled to the instruction and data paths and operable to decode and execute instructions received from the instruction

path" is described in the '599 patent at Fig. 1 and col. 4, lines 10-66, the '599 appendix at p. 363-83, and the '840 patent at Figures 6 and 7, and col. 11, line 19 through col. 12, line 15.

Regarding claim 10, the recited data processing system further comprising in part an execution unit "wherein in response to decoding a single instruction specifying both a mask and a register containing data, the mask comprising fields that each correspond to a field of the data contained in the register, the execution unit is operable to: (i) detect some of the fields of the mask as having a predetermined value and identifying corresponding fields of the data contained in the register as write-enabled data fields; and (ii) cause the write-enabled data fields to be written to a specified memory location" is described in the '599 appendix at p. 123-25 and 128-30, and the '840 appendix at p. 150-53 and 154-57.

Regarding claim 11, the recited data processing system "wherein each of the fields of the mask has a width of one bit" is described in the '599 appendix at p. 123-25 and 128-30, and the '840 appendix at p. 150-53 and 154-57.

Regarding claim 12, the recited data processing system "wherein each of the fields of the data contained in the register has a width of one bit" is described in the '599 appendix at p. 123-25 and 128-30, and the '840 appendix at p. 150-53 and 154-57.

Regarding claim 13, the recited data processing system "wherein the execution unit is operable to cause the write-enabled data fields to be written to the specified memory location by reading an unaltered field of data from the specified memory location and writing the unaltered field of data along with the write-enabled data fields to the specified memory location" is described in the '599 appendix at p. 123-25 and 128-30, and the '840 appendix at p. 150-53 and 154-57.

Regarding claim 14, the recited data processing system "wherein the mask is contained in a specified register" is described in the '599 appendix at p. 123-25 and 128-30, and the '840 appendix at p. 150-53 and 154-57.

Regarding claim 15, the recited data processing system "wherein the memory location is contained in a specified register" is described at pages is described in the '599 appendix at p. 123-25 and 128-30, and the '840 appendix at p. 150-53 and 154-57.

Regarding claim 16, the recited data processing system "wherein the specified memory location comprises a section of memory having a specific width and beginning at a specific memory address" is described at pages is described in the '599 appendix at p. 123-25 and 128-30, and the '840 appendix at p. 150-53 and 154-57.

Regarding claim 17, the recited data processing system "wherein the predetermined value is a logic 1" is described at pages is described in the '599 appendix at p. 123-25 and 128-30, and the '840 appendix at p. 150-53 and 154-57.

Regarding claim 18, the recited data processing system "wherein the execution unit is further operable to, in response to decoding a second single instruction specifying a third and a fourth register each containing a plurality of operands, multiply the plurality of floating point operands in the third register by the plurality of operands in the fourth register to produce a plurality of products and provide the plurality of products to partitioned fields of a result register as a second catenated result" is described in the '599 appendix at p. 258-60, and the '840 appendix at p. 129-31.

Support for New Claims 19-32

New claims 19-32 are fully supported by the present specification. Support for specific claim elements is identified below by citing to the present specification as published (United States Patent Publication Number US2004/0210746).

Regarding claim 19, a programmable processor comprising in part "a virtual memory addressing unit; an instruction path and a data path; an external interface operable to receive data from an external source and communicate the received data over the data path; a cache operable to retain data communicated between the external interface and the data path; a register file comprising a plurality of registers coupled to the data path; and an execution unit, coupled to the instruction and data paths, that is operable to decode and execute instructions received from the instruction path" is described at Fig. 1 and paragraphs 0078-85..

Regarding claim 19, the recited programmable processor further comprising in part an execution unit "wherein in response to decoding a single instruction specifying both a mask and a register containing data, the mask comprising fields that each correspond to a field of the data

contained in the register, the execution unit is operable to: (i) detect some of the fields of the mask as having a predetermined value and identifying corresponding fields of the data contained in the register as write-enabled data fields; and (ii) cause the write-enabled data fields to be written to a specified memory location" is described at Figures 52A-C and 53A-C, and paragraphs 0316-320.

Regarding claim 20, the recited programmable processor "wherein the first predetermined value is a logic 1" is described at Figures 52A-C and 53A-C, and paragraphs 0316-320.

Regarding claim 21, the recited programmable processor "wherein for each bit in the first operand, the bitwise insert operation maintains a corresponding bit position in the destination value as unchanged if a corresponding bit in the second operand has a second predetermined value" is described at Figures 52A-C and 53A-C, and paragraphs 0316-320.

Regarding claim 22, the recited programmable processor "wherein the second predetermined value is a logic 0" is described at Figures 52A-C and 53A-C, and paragraphs 0316-320.

Regarding claim 23, the recited programmable processor "wherein the bitwise insert operation stores the destination value into memory" is described in the '599 appendix at p. 123-25 and 128-30, and the '840 appendix at p. 150-53 and 154-57.

Regarding claim 24, the recited programmable processor "wherein each of the first and second operands has a width of 64 bits" is described at Figures 52A-C and 53A-C, and paragraphs 0316-320.

Regarding claim 25, the recited programmable processor "wherein the execution unit is further capable of executing a plurality of different group floating-point arithmetic operations that arithmetically operate on multiple floating-point operands stored in partitioned fields of an operand register in the plurality of registers to produce a catenated result that is returned to a register in the plurality of registers, wherein the catenated result comprises a plurality of individual floating-point results." is described at Figures 38A-C and 39A-C, and paragraphs 0236-37.

Regarding claim 26, a device having installed therein a programmable processor, the programmable processor comprising in part "a virtual memory addressing unit; an instruction path and a data path; an external interface operable to receive data from an external source and communicate the received data over the data path; a cache operable to retain data communicated between the external interface and the data path; a register file comprising a plurality of registers coupled to the data path; and an execution unit, coupled to the instruction and data paths, that is operable to decode and execute instructions received from the instruction path" is described at Figures 52A-C and 53A-C, and paragraphs 0316-320

Regarding claim 26, the recited device having installed therein a programmable processor, the programmable processor further comprising in part "the execution unit capable of performing a bitwise insert operation that operates on a first and a second operand stored in registers in the register file, wherein for each bit in the first operand, the bitwise insert operation inserts the bit into a corresponding bit position in a destination value if a corresponding bit from the second operand has a first predetermined value" is described at Figures 52A-C and 53A-C, and paragraphs 0316-320.

Regarding claim 27, the recited device "wherein the first predetermined value is a logic 1" is described at Figures 52A-C and 53A-C, and paragraphs 0316-320.

Regarding claim 28, the recited device "wherein for each bit in the first operand, the bitwise insert operation maintains a corresponding bit position in the destination value as unchanged if a corresponding bit in the second operand has a second predetermined value" is described at Figures 52A-C and 53A-C, and paragraphs 0316-320.

Regarding claim 29, the recited device "wherein the second predetermined value is a logic 0" is described at Figures 52A-C and 53A-C, and paragraphs 0316-320.

Regarding claim 30, the recited device "wherein the bitwise insert operation stores the destination value into memory" is described at Figures 52A-C and 53A-C, and paragraphs 0316-320.

Regarding claim 31, the recited device "wherein each of the first and second operands has a width of 64 bits" is described at Figures 52A-C and 53A-C, and paragraphs 0316-320.

Regarding claim 25, the recited device "wherein the execution unit is further capable of executing a plurality of different group floating-point arithmetic operations that arithmetically operate on multiple floating-point operands stored in partitioned fields of an operand register in the plurality of registers to produce a catenated result that is returned to a register in the plurality of registers, wherein the catenated result comprises a plurality of individual floating-point results." is described at Figures 38A-C and 39A-C, and paragraphs 0236-37.

Conclusion

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Michael A. Messina
Registration No. 33,424

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MAM:DAB
Facsimile: 202.756.8087
Date: November 15, 2006

Please recognize our Customer No. 20277 as our correspondence address.

Docket No.: 43876-155 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Craig HANSEN, et al.	:	Confirmation Number: To be assigned
Serial No.: Unknown	:	Group Art Unit: To be assigned
Continuation of Application No. 10/646,787 Filed August 25, 2003	:	
Filed: January 15, 2004	:	Examiner: To be assigned

For: **PROGRAMMABLE PROCESSOR AND SYSTEM FOR STORE MULTIPLEX OPERATION**

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Mail Stop NEW APPLICATION
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached form PTO-1449. It is respectfully requested that the documents be expressly considered during the prosecution of this application, and that the documents be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

The references were cited by or submitted to the U.S. Patent and Trademark Office in parent application in Serial No. 10/646,787, filed August 25, 2003, which is relied upon for an earlier filing date under 35 USC 120. thus copies of these references are not attached. 37 CFR 1.98(d)

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Lawrence T. Cullen
Registration No. 44,489

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 LTC:BD
Facsimile: (202) 756-8087
Date: January 15, 2004

WDC99 864105-1.043876.0155

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(PTO-1449)

ATTY. DOCKET NO.	SERIAL NO.
43876-155	**Continuation of Serial No. 10/646,787**
APPLICANT: **Craig HANSEN, et al.**	
FILING DATE: **January 15, 2004**	GROUP: **To be assigned**

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code2 (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US	4,785,393	11/15/1988	Chu et al.	
		US	4,814,976	03/21/1989	Craig C. Hansen, et al.	
		US	5,031,135	07/09/1991	Patel	
		US	5,280,598	01/1994	Osaki et al.	
		US	5,481,686	01/02/1996	Dockser	
		US	5,487,024	01/1996	Girardeau Jr.	
		US	5,600,814	02/1997	Gahan et al.	
		US	5,740,093	04/14/1998	Sharangpani	
		US	5,742,840	04/21/1998	Hansen et al.	
		US	5,768,546	06/1998	Kwon	
		US	5,898,849	04/27/1999	Tran	
		US	5,996,057	11/30/1999	Hunter L. Scales, III, et al.	
		US	6,041,404	03/21/2000	Patrice Roussel, etla.	
		US	6,052,769	04/18/2000	Thomas R. Huff, et al	
		US	6,173,393 B1	01/09/2001	Salvador Palanca, et al.	
		US	6,275,834 B1	08/14/2001	Derrick Chu Lin, et al	
		US	6,295,599	09/2001	Hansen et al.	

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes-Number 4-Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes	Translation No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
		IEEE Draft Standard for "Scalable Coherent Interface-Low-Voltage Differential Signal Specifications And Packet Encoding", IEEE Standards Department, P1596.3/D0.15 (March 1992)	
		IEEE Draft Standard for "High-Bandwidth Memory Interface Based on SCI Signaling Technology (RamLink)", IEEE Standards Department, Draft 1.25 IEEE P1596.4-199X (May 1995)	
		IBM, "The PowerPC Architecture: A Specification For A New Family of Risc Processors", 2nd Ed., Morgan Kaufmann Publishers, Inc., (1994).	
		Hewlett-Packard Co., "PA-RISC 1.1 Architecture and Instruction Set", Manual Part No. 09740-90039, (1990).	
		MIPS Computer Systems, Inc., "MIPS R4000 User's Manual", Mfg. Part No. M8-00040, (1990).	

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

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Craig HANSEN, et al.	:	Confirmation Number: To be assigned
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SECOND SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

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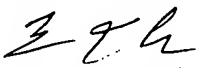
Respectfully submitted,

MCDERMOTT, WILL & EMERY



Lawrence T. Cullen
Registration No. 44,489

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Washington, DC 20005-3096
(202) 756-8000 LTC:BD
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WDC99 866034-1.043876.0155

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

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		US	5,819,101	10/6/1998	Alexander Peleg, et al	
		US	5,881,275	3/9/1999	Alexander Peleg, et al	
		US	6,119,216	9/12/2000	Alexander Peleg, et al	
		US	6,516,406	2/4/2003	Alexander Peleg, et al	
		US	6,539,467	3/25/2003	Timothy D. Anderson, et al	
		US	6,574,724	6/3/2003	David Hoyle, et al	
		US	6,631,389 B2	10/7/2003	Derrick Chu Lin, et al	
		US				
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FOREIGN PATENT DOCUMENTS

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EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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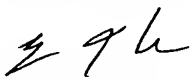
MCDERMOTT, WILL & EMERY



Lawrence T. Cullen
Registration No. 44,489

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 LTC:BD
Facsimile: (202) 756-8087
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INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(PTO-1449)

ATTY. DOCKET NO.	SERIAL NO.
43876-155	**Continuation of Serial No. 10/646,787**
APPLICANT: **HANSEN, et al.**	
FILING DATE: **January 15, 2004**	GROUP: **To be assigned**

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
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EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)	ATTY. DOCKET NO. 43876-155	SERIAL NO. Continuation of Serial No. 10/646,787
	APPLICANT HANSEN, et al.	
	FILING DATE January 15, 2004	GROUP To be assigned

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EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No

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Applicant: Craig HANSEN, et al. Docket No. 43876-155

Title: PROGRAMMABLE PROCESSOR AND SYSTEM FOR STORE MULTIPLEX OPERATION Serial/Reg./Patent No. Cont. of 10/646,787

Date Sent: 1/15/2004 ☒ Hand Carried ☐ Fax ☐ Electronic ☐ Cert. of Mailing ☐ Express Mail No.

☒ Transmittal Letter

New Patent App ☐ Utility ☐ Design ☒ Cont. ☐ CIP ☐ Div. ☐ PCT ☐ RCE ☐ Prov

☐ Other:

76 pages of Specification

4 pages of Claims

1 pages of Abstract

152 pages of Formal/Informal Drawings

☐ Small Entity ☒ Large Entity

☒ Declaration/ 2 COPIES

☐ Recordation of Assignment/Security Agreement

☒ Information Disclosure Statement

3 Form PTO 1449

copies of cited references

☐ Preliminary Amendment

☐ Response to Missing Parts Notice

☐ Resp. to Notice to Correct App. Papers

☐ Certified Copy of Priority Doc.

☐ Claim for Convention Priority

☐ Response/Amendment to Office Action of

☐ Request for month Extension of Time

☐ Letter submitting pages of drawings

☐ Req. for Approval of Drawing Amendments

☐ Req. for Oral Hearing

☐ Not. of Appeal ☐ Appeal Brief ☐ Reply Brief

☐ Rule 312 Amendment/Letter

☐ Req. for Acknowledgement of Cited Art

☐ Issue Fee

☐ Publication Fee

☐ Req. for Certificate of Correction

☐ Maintenance Fee for years after grant

☐ Fee Address Indication Form

☐ Terminal Disclaimer

☐ Petition to Commissioner

☐ Status Inquiry

☒ Other Suppl. IDS , 1-pg 1449, 2.Supp. IDS & 7 refs

OIPE JC34 JAN 15 2004 PATENT & TRADEMARK OFFICE

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